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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/591,615	06/09/2000	Laurent Six	TI-29030	2796

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EXAMINER
BATAILLE, PIERRE MICHE

ART UNIT	PAPER NUMBER
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/591,615	SIX ET AL.	
	Examiner	Art Unit	
	Pierre-Michel Bataille	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-10 are presented for examination in the application. Acknowledged is made of claim of priority based on foreign application #99401388.6 filed in Europe on June 9, 1999.

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. The following objections noted are merely exemplary, Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The disclosure is objected to because of the following informalities:
On page 1, lines 10-13, and throughout the specification, the specification should be amended to replace all "Attorney Docket No." with the current application serial number and update the status of all related applications (see page 1, lines 4-5 and page 10, line 16). See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 8-10 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,638,530 (Pawate et al).

With respect to claim 8, Pawate teaches a system and method operating a digital system having a memory circuit (*smart card*) that is shared by a plurality of requestors circuits (*digital signal processor 170 and host computer 200*) [Fig. 2] comprising: sharing access to the memory circuit (smart card) between the plurality of requestors circuits (*digital signal processor 170 and host computer 200*) when the digital system in a first mode of operation (*standard mode*) [Col. 13, Lines 53-65; Col. 14, Lines 32-41]; selecting a portion of the memory (*attribute memory 160 of the smart card*) responsive to a size parameter stored in a register (*interface configuration registers 130*) [Col. 4, Lines 53-65], such that the second portion is not selected (*common memory 150 of the smart card*) [Col. 7, Lines 36-42]; and limiting access (*smart mode*) to the first portion of the memory circuit (*attribute memory 160 of the smart card*) to only a first requestor (*digital signal processor (DSP) 170*) in a second mode of operation (smart mode) [Col. 13, Lines 53-65; Col. 14, Lines 32-41; Col. 7, Lines 22-42, Col. 7, Line 61 to Col. 8, Line 2].

With respect to claim 9, Pawate teaches sharing access to the second portion of the memory circuit between the plurality of requester circuits when the digital system is in the second mode of operation [Col. 13, Lines 53-65; Col. 14, Lines 32-41].

With respect to claim 10, Pawate teaches placing the second portion of the memory circuit in a low power mode when the digital system is in the second

mode of operation *(minimizing power consumption of the smart card while in the smart mode until an external event, allowing the host computer to have quicker access to the remaining unused portion on the card)* [Col. 9, Lines 53-56; Col. 14, Lines 3-13].

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,838,934 (Boutaud et al) in view of US 5,638,530 (Pawate et al)

With respect to claim 1, Pawate teaches a system and method operating a digital system having a memory circuit (*smart card*); a plurality of requestors circuits including first requester circuit with a first access node (*digital signal processor 170*) and a second requester circuit with a second access node (*host computer 200*) [Fig. 2]; a scheduling circuit (*PC/DSP bus arbitration circuit 120*) connected to the first access node and to the second access node operable to sequentially schedule memory access to the memory circuit by the first and second requester circuit [Col. 13, Lines 29-33; Col. 3, Lines 18-20]; and access mode circuitry for:

sharing access to the memory circuit (smart card) between the plurality of requestors circuits (*digital signal processor (DSP) 170 and host computer 200*) when the

digital system in a first mode of operation (*standard mode*) [Col. 13, Lines 53-65; Col. 14, Lines 32-41];

selecting a portion of the memory (*attribute memory 160 of the smart card*) responsive to a size parameter stored in a register (*interface configuration registers 130*) [Col. 4, Lines 53-65], such that the second portion is not selected (*common memory 150 of the smart card*) [Col. 7, Lines 36-42]; and limiting access (*smart mode*) to the first portion of the memory circuit (*attribute memory 160 of the smart card*) to only a first requestor (*host computer 200*) in a second mode of operation (smart mode) [Col. 13, Lines 53-65; Col. 14, Lines 32-41; Col. 7, Lines 22-42, Col. 7, Line 61 to Col. 8, Line 2].

Pawate fails to specifically teach a selection circuit connected to the scheduling circuit request output node with an output node connected to the memory circuit. Although this features would be inherent in Pawate's disclosure, Boutaud teaches a selection circuit (multiplexer 111, 113, 121, 123 and 160) connected to first memory access node (host port internal data and address 110 to mux (111, 113, 121, and 123) and control bus 138c to mux 160) and to a scheduling circuit request output node (synchronizer logic with output line 136, 146) with an output node connected to the memory circuit (output line 115c, 116c, 122a, 124a connected to the memory via memory interface logic 140, which provides the address, data and control via address, data and control line 148a, 148d, and 148c) [Col. 5, Lines 14-26; Col. 6, Lines 8-14]; wherein control logic is used to determine the type of access (Col. 10, Lines 48-51; Col. 8, Lines 28-31), shared access mode (SAM) or host only mode (HOM) (Col. 12, Lines 32-36) where control logic 130a generates memory control synchronous

memory control signals when shared access mode is required (Col. 9, Lines 1-18)], such that both the first requester circuit and the second requester circuit can sequentially access the memory circuit when the priority circuitry indicates a first relative priority state between the first priority and the second priority (Col. 13, Lines 25-40); when in shared access mode (SAM) access by both the host 400 and the processor 300 are synchronized to clock signals to avoid conflicts (Col. 8, Lines 63-67; Col. 16, Lines 14-21; Col. 8, Lines 59-63: Col. 16, Lines 22-27].

Therefore, it would have been obvious to one having ordinary skill in the art and having both teaches before him at the time of the invention, to combine the selection feature of claim Boutaud with the digital signal processing system of Pawate because the selection feature would have provided control using either synchronous or asynchronous clock signal to portion of the memory circuit for selectively providing selectively accessible by first type of requestor and second type of requestor, as taught by Boutaud Col. 2, Lines 18-31].

With respect to claim 2, Pawate teaches placing the second portion of the memory circuit in a low power mode when the digital system is in the second mode of operation *(minimizing power consumption of the smart card while in the smart mode until an external event, allowing the host computer to have quicker access to the remaining unused portion on the card)* [Col. 9, Lines 53-56; Col. 14, Lines 3-13].

With respect to claim 3, Pawate teaches the second portion of the memory circuit, not selected in response to the size parameter can be accessed by the

second requester when the access mode indicates the second mode of access [Col. 13, Lines 53-65].

With respect to claim 4, Pawate teaches the indication of first access mode such that the entire memory is operable to be selected for sequential access by the first requester and the second requestor [Col. 13, Lines 29-48].

With respect to claim 5, Pawate teaches clock circuit connected to the DSP and the memory circuit wherein the first portion of the memory operates synchronously with the clock circuit in the first mode of access and wherein the first portion of the memory operated asynchronously in the second mode of access [Col. 13, Lines 62-65; Col. 14, Lines 2-42]; Boutaud additionally teaches sharing access to the memory circuit between the plurality of requestor circuits (shared access mode (SAM Mode when in shared access mode (SAM), accesses by both the host 400 and the processor 300 are synchronized with clock signals and provided sequentially to avoid conflicts) [Col. 8, Lines 63-67; Col. 16, Lines 14-21] and limiting scheduling accesses to one of the requester with no need to synchronize host accesses with the processor clock signals (bypassing the synchronizer logic 130c in host only mode (HOM) Col. 8, Lines 59-63; Col. 16, Lines 22-27].

With respect to claims 6 and 7, Pawate teaches the system wherein the first requestor is a host processor and the second requester is a direct memory access circuit channel controller [Fig. 1]; and the system being a digital signal processing system comprising an integrated keyboard provided with keyboard

adapter, a display, radio frequency and an aerial connected with the radio frequency [inherent in all cellular telephone; Fig. 1 and Fig. 2].

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 6,122,713 (Huang et al) teaching dual port shared memory system including semaphore for high priority and low Priority requestors.

US 6,119,003 (Kukkohovi) teaching method and apparatus for performing automatic mode selection in a multimode mobile terminal.

US 5,922,047 (Newlin et al) teaching apparatus and method for apparatus, method and system for multimedia control in a processor arrangement having a plurality of operating modes.

US 5,218,686 (Thayer) teaching combined synchronous and asynchronous memory controller where the sysnchronous portion is used when the system processor is accessing the memory.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (703) 305-0134. The examiner can normally be reached on Tue-Fri (7:30A to 6:00P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (703) 305-3821. The

fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Pierre-Michel Bataille
Examiner
Art Unit 2186

January 22, 2003